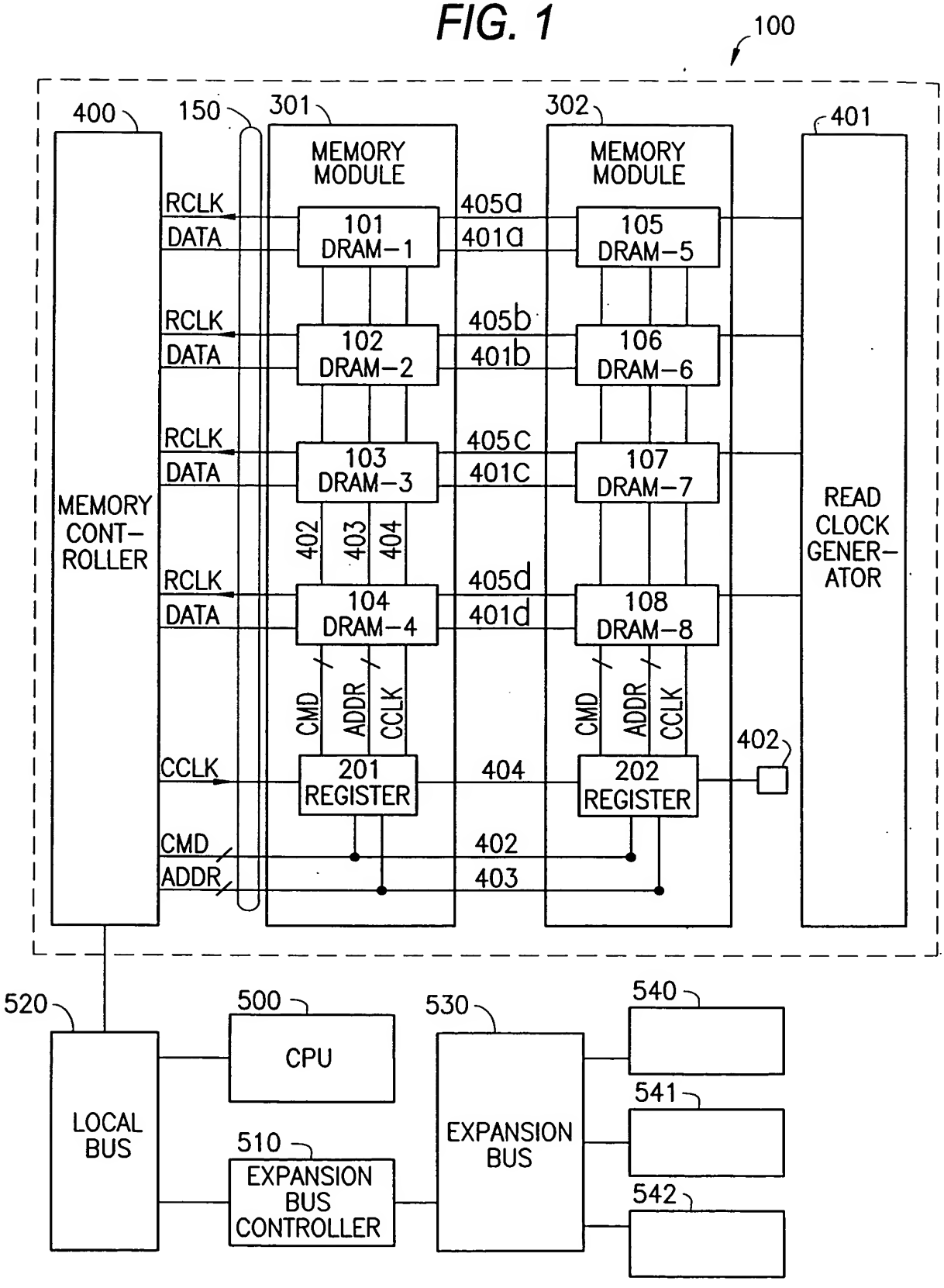
FIG. 1


100
400
150
301
302
401
MEMORY MODULE
MEMORY MODULE
RCLK
DATA
101 DRAM-1
105 DRAM-5
405a
401a
102 DRAM-2
106 DRAM-6
405b
401b
103 DRAM-3
107 DRAM-7
405c
401c
104 DRAM-4
108 DRAM-8
405d
401d
MEMORY CONT-ROLLER
READ CLOCK GENER-ATOR
402
403
404
CMD
ADDR
CCLK
201 REGISTER
202 REGISTER
CCLK
CMD
ADDR
520
500
530
540
541
542
CPU
LOCAL BUS
EXPANSION BUS
510
EXPANSION BUS CONTROLLER

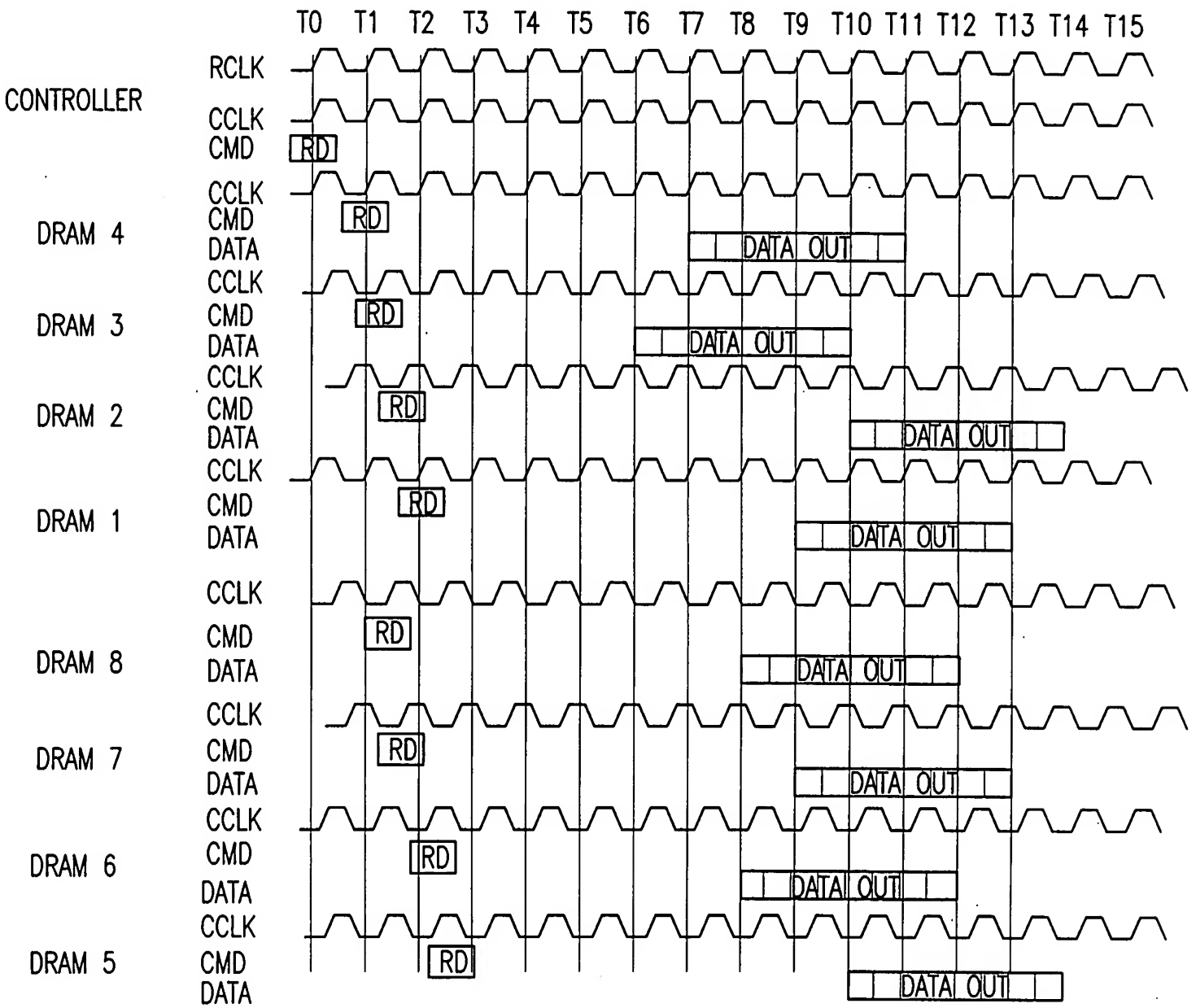

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15
CONTROLLER
RCLK
CCLK
CMD
RD
CCLK
DRAM 4
CMD
DATA
RD
DATA OUT
CCLK
DRAM 3
CMD
DATA
RD
DATA OUT
CCLK
DRAM 2
CMD
DATA
RD
DATA OUT
CCLK
DRAM 1
CMD
DATA
RD
DATA OUT
CCLK
DRAM 8
CMD
DATA
RD
DATA OUT
CCLK
DRAM 7
CMD
DATA
RD
DATA OUT
CCLK
DRAM 6
CMD
DATA
RD
DATA OUT
CCLK
DRAM 5
CMD
DATA
RD
DATA OUT

FIG. 2

FIG. 3A

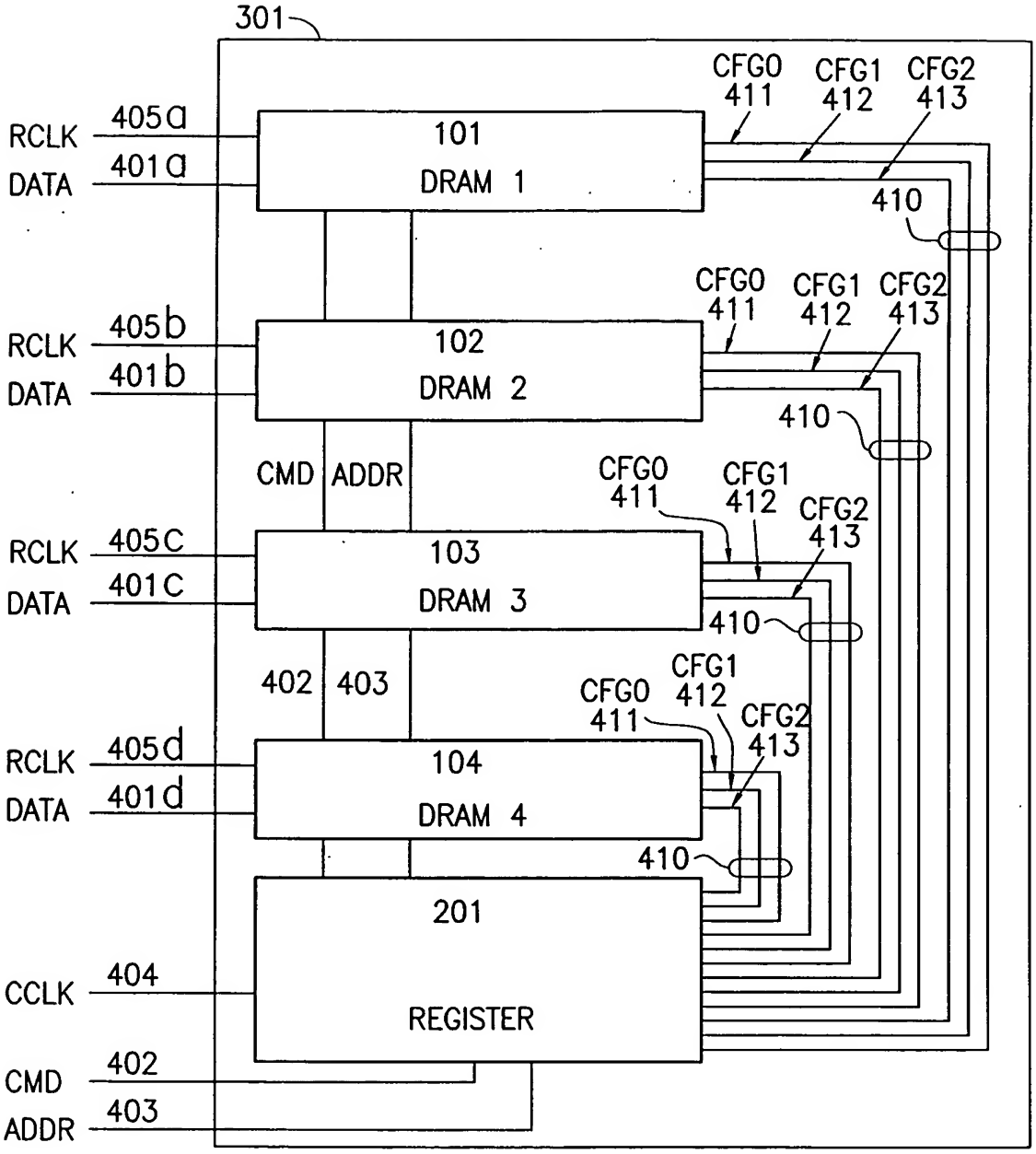

301
CFG0 411
CFG1 412
CFG2 413
RCLK
DATA
405a
401a
101
DRAM 1
410
405b
401b
102
DRAM 2
CMD
ADDR
405c
401c
103
DRAM 3
402
403
405d
401d
104
DRAM 4
201
REGISTER
CCLK
404
CMD
402
ADDR
403

FIG. 3B

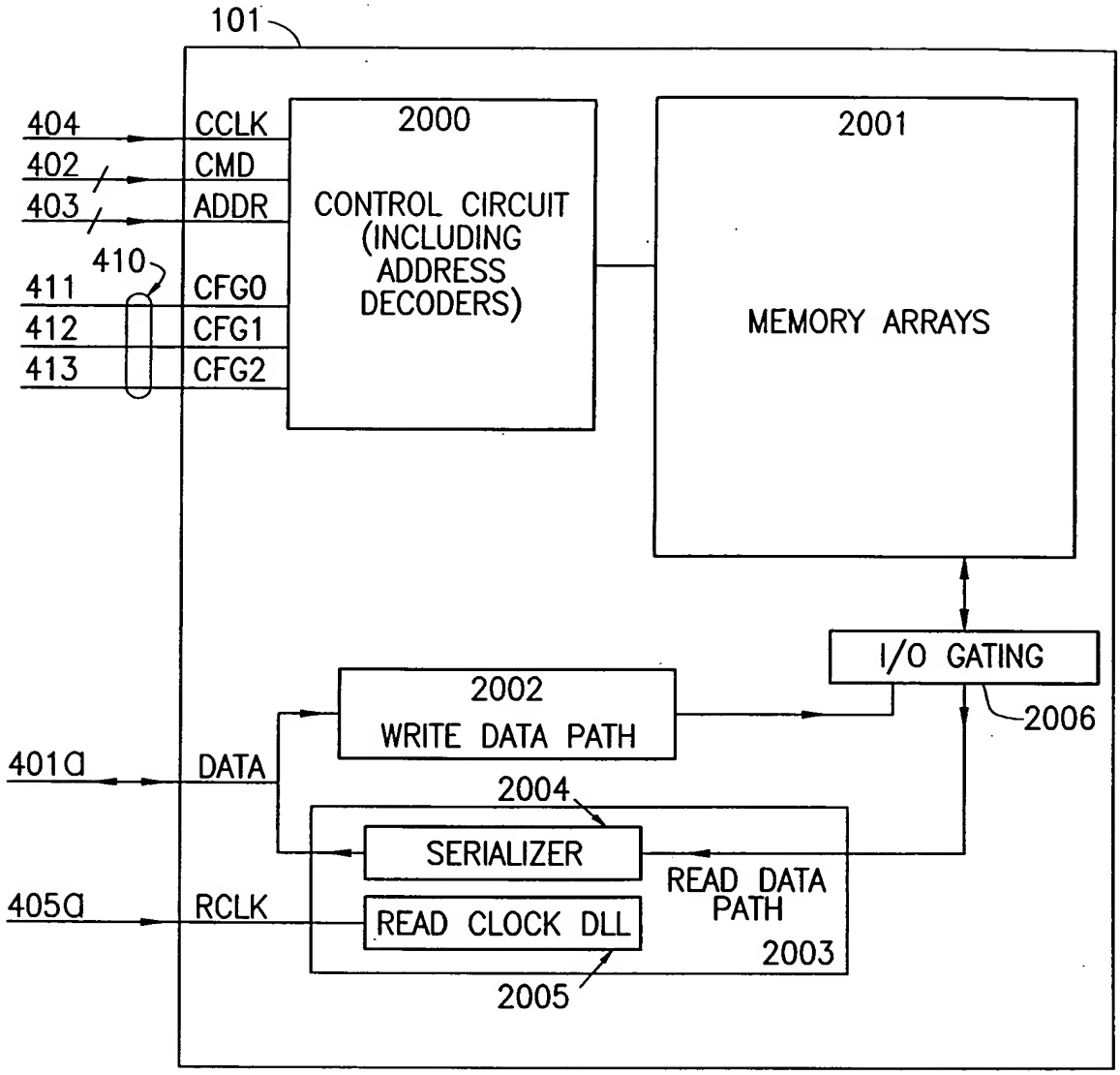
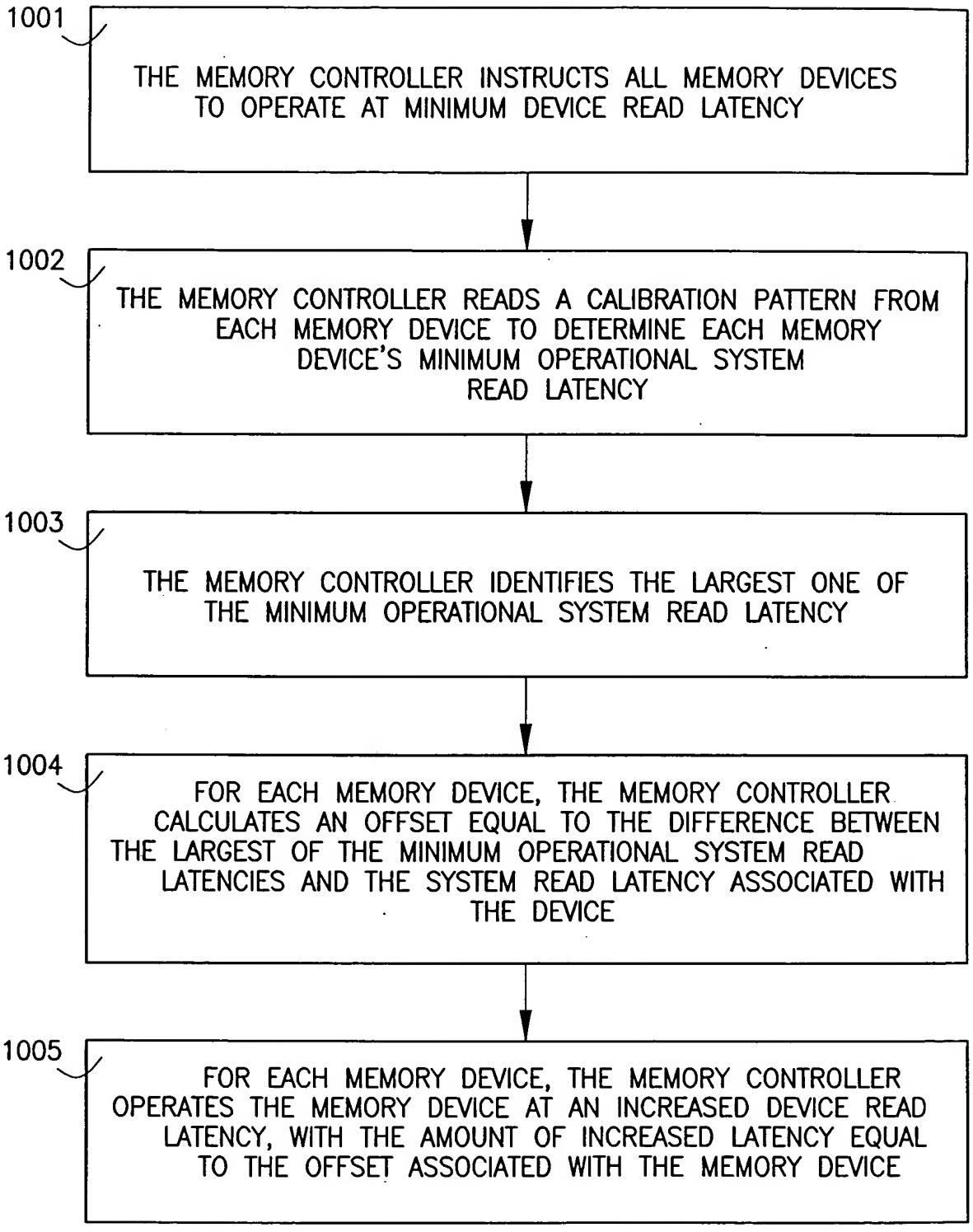

101
404
CCLK
402
CMD
403
ADDR
410
411
CFG0
412
CFG1
413
CFG2
2000
CONTROL CIRCUIT (INCLUDING ADDRESS DECODERS)
2001
MEMORY ARRAYS
I/O GATING
2006
2002
WRITE DATA PATH
401a
DATA
2004
SERIALIZER
READ DATA PATH
2003
405a
RCLK
READ CLOCK DLL
2005

FIG. 4

DEVICE READ LATENCY	CFG2	CFG1	CFG0
MINIMUM DEVICE READ LATENCY	0	0	0
MINIMUM DEVICE READ LATENCY + 1 CLOCK CYCLE	0	0	1
MINIMUM DEVICE READ LATENCY + 2 CLOCK CYCLES	0	1	0
MINIMUM DEVICE READ LATENCY + 3 CLOCK CYCLES	0	1	1
MINIMUM DEVICE READ LATENCY + 4 CLOCK CYCLES	1	0	0
MINIMUM DEVICE READ LATENCY + 5 CLOCK CYCLES	1	0	1
MINIMUM DEVICE READ LATENCY + 6 CLOCK CYCLES	1	1	0
MINIMUM DEVICE READ LATENCY + 7 CLOCK CYCLES	1	1	1

FIG. 5


1001
THE MEMORY CONTROLLER INSTRUCTS ALL MEMORY DEVICES TO OPERATE AT MINIMUM DEVICE READ LATENCY
1002
THE MEMORY CONTROLLER READS A CALIBRATION PATTERN FROM EACH MEMORY DEVICE TO DETERMINE EACH MEMORY DEVICE'S MINIMUM OPERATIONAL SYSTEM READ LATENCY
1003
THE MEMORY CONTROLLER IDENTIFIES THE LARGEST ONE OF THE MINIMUM OPERATIONAL SYSTEM READ LATENCY
1004
FOR EACH MEMORY DEVICE, THE MEMORY CONTROLLER CALCULATES AN OFFSET EQUAL TO THE DIFFERENCE BETWEEN THE LARGEST OF THE MINIMUM OPERATIONAL SYSTEM READ LATENCIES AND THE SYSTEM READ LATENCY ASSOCIATED WITH THE DEVICE
1005
FOR EACH MEMORY DEVICE, THE MEMORY CONTROLLER OPERATES THE MEMORY DEVICE AT AN INCREASED DEVICE READ LATENCY, WITH THE AMOUNT OF INCREASED LATENCY EQUAL TO THE OFFSET ASSOCIATED WITH THE MEMORY DEVICE

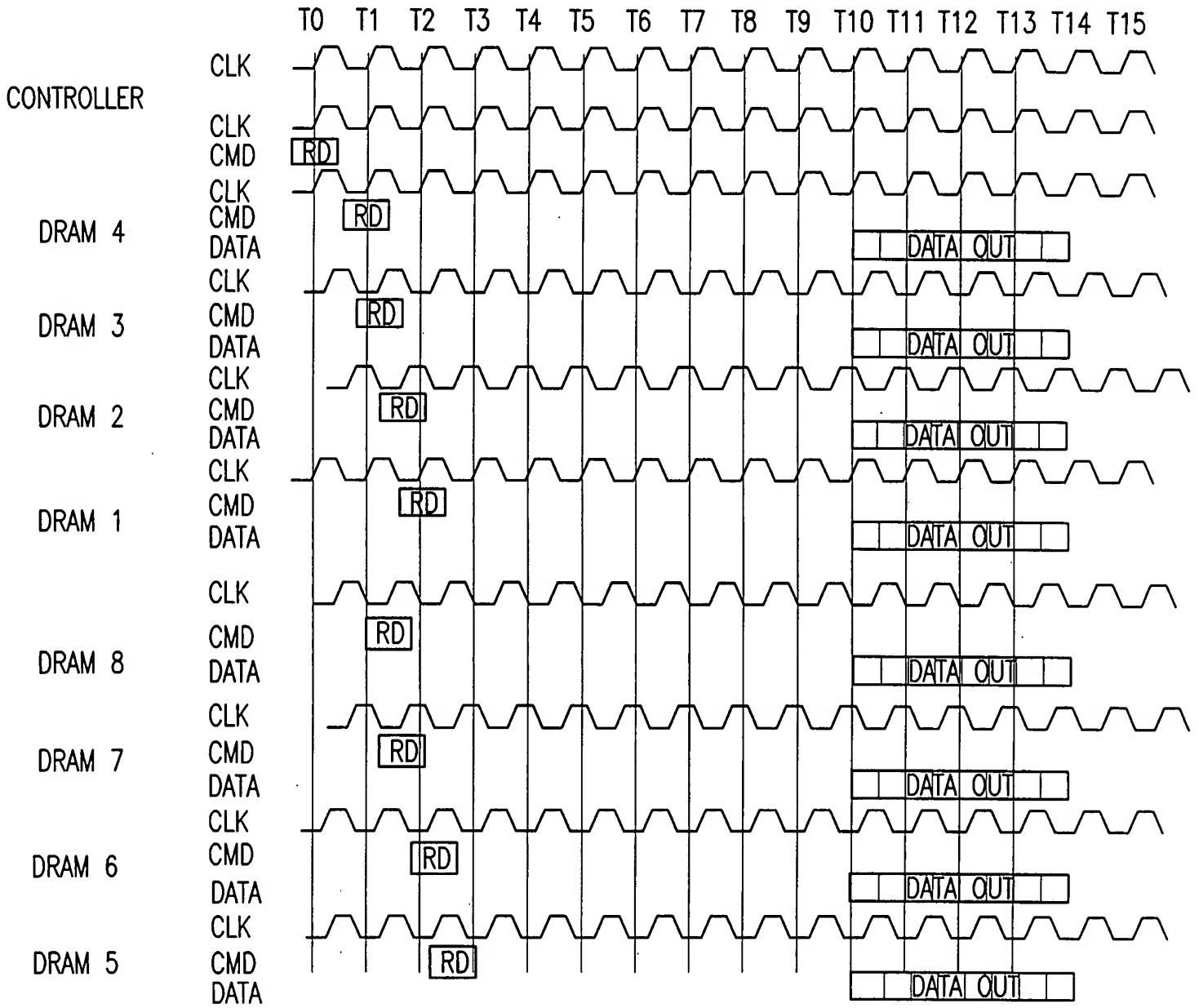

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15
CONTROLLER
CLK
CLK
CMD
RD
CLK
DRAM 4
CMD
RD
DATA
DATA OUT
CLK
DRAM 3
CMD
RD
DATA
DATA OUT
CLK
DRAM 2
CMD
RD
DATA
DATA OUT
CLK
DRAM 1
CMD
RD
DATA
DATA OUT
CLK
DRAM 8
CMD
RD
DATA
DATA OUT
CLK
DRAM 7
CMD
RD
DATA
DATA OUT
CLK
DRAM 6
CMD
RD
DATA
DATA OUT
CLK
DRAM 5
CMD
RD
DATA
DATA OUT

FIG. 6